REMARKS/ARGUMENTS

Information Disclosure Statement

Applicant submitted an Information Disclosure Statement (IDS) on 12/10/2004 in relation to the present application. A copy of the original IDS and accompanying transmittal letter are attached. Thus far in the prosecution of the present application, the Examiner has not indicated that she has considered the references contained in the IDS. Applicant respectfully requests the Examiner to include in the next Office Action an initialed version of the IDS indicating the Examiner has considered the references contained in the IDS. Applicant further notes that additional IDS's have been submitted in the meantime, and respectfully requests the Examiner consider them as well.

In the Office Action, the Examiner noted that claims 1-30, 34-39 and 45-50 are pending in the application. The Examiner additionally stated that claims 1-30, 34-39 and 45-50 are rejected. By this amendment, claims 1, 6, 8-10, 12, 15, 22, 24-25, 28, 36, 39, 45, and 48 have been amended, and new claims 51-77 have been added. Hence, claims 1-43 and 45-77 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Specification

In the specification, the table on page 1 has been amended to identify the co-pending applications by their serial numbers.

In the Claims

Rejections Under 35 U.S.C. §103(a)

The Examiner rejected claims 1, 2, 15-30, 34-39, 45, 48, and 50 under 35 U.S.C. 103(a) as being unpatentable over Emma et al., U.S. Patent No. 5,353,421 (hereinafter *Emma*) in view of Hughes et al., U.S. Patent No. 4,200,927 (hereinafter *Hughes*). Applicant respectfully traverses the Examiner's rejections.

First a discussion of *Emma* and *Hughes* is helpful. *Emma* and *Hughes* are directed to the IBM System/370 processor. See for example, *Emma*: col. 13, line 9-10; *Hughes*: col. 1, lines 14-17, col. 6, lines 12-20, col. 10, lines 62-66, col. 11, lines 46-50. *Emma* specifically states that neither the branch prediction mechanism of *Hughes* nor the DHT of Losq et al. (the DHT employed by *Emma*) attempt to guess the target address of the branch instruction since in the IBM System/370 processor the target address is precisely known when the branch instruction is discovered and decoded at the decode stage of the pipeline. *Emma*, col. 3, lines 28-40. In other words, neither *Hughes*' branch predictor nor *Emma*'s DHT makes a prediction of a branch instruction target address. Rather, *Hughes*' branch predictor and *Emma*'s DHT make a prediction of a conditional branch instruction outcome (also commonly referred to as a branch instruction direction, i.e., whether a conditional branch instruction will be taken or not taken), not a prediction of a target address of a branch instruction. See *Emma*: col. 3, lines 32-36, col. 6, lines 23-25, col. 5, lines 40-53, col. 1, line 59 to col. 2, line 1; *Hughes*: Abstract; col. 3, lines 1-3; col. 10, line 66 to col. 11, line 2; col. 12, lines 15-18; col. 13, lines 58-67 (*Hughes* more often uses the terms "successful" and "unsuccessful" for taken and not taken).

With respect to claim 1, the Examiner states that *Hughes* has taught an op-code type branch predictor that may be substituted for the DHT of *Emma* to result in two branch predictions for unconditional branch instructions. However, claim 1 recites not merely branch predictions, but specifically branch instruction target address predictions. As discussed above, neither *Emma*'s DHT nor *Hughes*' branch predictor provides a prediction of a target address of a branch instruction. That is, neither *Emma*'s DHT nor *Hughes*' branch predictor provides a target address of a branch instruction that has the possibility of being the incorrect target address of the branch instruction. Although *Emma*'s DHT and *Hughes*' branch predictor provide an outcome prediction (taken/not taken) that has the possibility of being incorrect, *Emma*'s address generate function (Fig. 10, element 19; col. 9, lines 13-24; col. 16, lines 45-51) and *Hughes* address formulation logic (Fig. 2, element 29; col. 6, lines 12-21, 40-41; col. 10, line 62 to col. 11, line 7) always generate the correct target address regardless of whether the direction prediction is correct or incorrect. Consequently, neither *Emma*'s DHT nor *Hughes*' branch predictor

teach a branch predictor that provides a target address prediction, which is a limitation recited by claim 1.

Furthermore, although *Emma* teaches a branch prediction mechanism that makes two predictions of conditional branch instructions, the two predictions (one by the BHT and one by the DHT) are of the outcome of the branch instruction, not of the target address of the branch instruction. That is, *Emma*'s branch prediction mechanism only makes one prediction of the target address of a branch instruction (by the BHT), whereas the second target address generated by *Emma*'s address generate function and compared with the BHT target address is always a correct target address, as discussed above.

For these reasons, Applicant respectfully requests that the Examiner withdraw the rejection to amended claim 1.

The Examiner rejected independent claims 28, 36 and 45 for the same reasons set forth in the rejection of claim 1. Claims 28 and 45 each recite the limitation of two target address predictions, and claim 36 has been amended to recite the limitation of two target address predictions. Thus, for the reasons discussed above with respect to claim 1, Applicant respectfully requests that the Examiner withdraw the rejection to claims 28, 36 and 45.

With respect to claims 2-27, 29-35 and 71-73, 37-43, and 46-50, these claims depend from independent claims 1, 28, 36, and 45, respectively, and add further limitations that are not obviated by *Emma* in view of *Hughes*. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejections to claims 2-27, 29-35 and 71-73, 37-43, and 46-50.

With respect to new claim 51, as discussed above with respect to claim 1, neither *Emma* nor *Hughes*, alone or in combination, teach generating first and second predictions of a target address of a branch instruction. Furthermore, neither *Emma* nor *Hughes*, alone or in combination, teach generating the second prediction of the target address based on the type of the branch instruction, after determining the type of the branch instruction. Still further, neither *Emma* nor *Hughes*, alone or in combination, teach if the first target address prediction does not match the second target address prediction and if the type of the branch instruction is a first of a plurality of predetermined types, branching

instruction fetching to the second target address prediction to override the branching to the first target address prediction. Additionally, neither *Emma* nor *Hughes*, alone or in combination, teach if the first target address prediction does not match the second target address prediction and if the type of the branch instruction is a second of the plurality of predetermined types, foregoing overriding the branching to the first target address prediction.

With respect to new claims 52-60, these claims depend from independent claim 51 and add further limitations that are not obviated by *Emma* in view of *Hughes*. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejections to claims 52-60.

With respect to new claim 61, as discussed above with respect to claim 1, neither *Emma* nor *Hughes*, alone or in combination, teach a first branch predictor that generates a first prediction of a target address of a branch instruction, a second branch predictor that generates a second prediction of the target address if the type of the branch instruction is a first of a plurality of predetermined types, and a third branch predictor that generates the second prediction of the target address of the branch instruction if the type of the branch instruction is a second of the plurality of predetermined types. Furthermore, neither *Emma* nor *Hughes*, alone or in combination, teach if the first target address prediction does not match the second target address prediction and if the type of the branch instruction is a first of the plurality of predetermined types, instruction fetch logic fetches a third cache line from the instruction cache at the second target address prediction to override the first branch predictor. Still further, neither *Emma* nor *Hughes*, alone or in combination, teach if the first target address prediction does not match the second target address prediction and if the type of the branch instruction is a second of the plurality of predetermined types, the instruction fetch logic foregoes overriding the first branch predictor.

With respect to new claims 62-70, these claims depend from independent claim 61 and add further limitations that are not obviated by *Emma* in view of *Hughes*. Accordingly,

Applicant respectfully requests that the Examiner withdraw the rejections to claims 62-70.

With respect to new claim 74, as discussed above with respect to claim 1, neither *Emma* nor *Hughes*, alone or in combination, teach a branch target address cache that provides a speculative target address prediction of a branch instruction and a target address calculator and a target address calculator that calculates a non-speculative target address prediction of the branch instruction. Furthermore, neither *Emma* nor *Hughes*, alone or in combination, teach a comparator that compares the speculative and non-speculative target address predictions. Finally, neither *Emma* nor *Hughes*, alone or in combination, teach the processor branching to the speculative target address prediction, and subsequently branching to the non-speculative target address prediction if the speculative and non-speculative target address predictions miscompare and if the instruction is a type in a first set of instruction types.

CONCLUSIONS

In view of the arguments advanced above, Applicant respectfully submits that claims 1-30, 34-39, and 45-77 are in condition for allowance. Reconsideration of the rejections is requested, and allowance of the claims is solicited.

Applicant earnestly requests that the Examiner contact the undersigned practitioner by telephone if the Examiner has any questions or suggestions concerning this amendment, the application, or allowance of any claims thereof.

Respectfully submitted,

/E. Alan Davis/

By:_____

E. ALAN DAVIS
Registration No. 39,954
Tel: (512) 301-7234

4/25/2006

Date: _____

Attachments (IDS previously submitted on 12/10/2004 but not considered)

In re application of:	G. Glenn Henry; Thomas C. McDonald
Serial No.:	09/849799
Filed:	05/04/01
Docket:	CNTR.2052
For:	SPECULATIVE BRANCH TARGET ADDRESS CACHE WITH SELECTIVE OVERRIDE BY SECONDARY PREDICTOR BASED ON BRANCH INSTRUCTION TYPE

INFORMATION DISCLOSURE STATEMENT SUBMITTED UNDER 37 CFR 1.97(D) AND 1.97 (E)(2)

Attached hereto is Form PTO-1449 listing documents believed relevant to the subject application. It is respectfully requested that the Examiner review the information disclosed herein in detail, independently evaluate each item carefully in the consideration of the pending claims and return an initialed copy of each form to the undersigned.

This disclosure statement should not be construed as a representation that a search has been made, that no other material information as defined in 37 C.F.R. § 1.56(a) exists, or as an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 CFR § 1.56(b) or is available as a reference under 35 U.S.C. § 102 *et seq.* Applicant reserves the right to swear behind or otherwise disprove the alleged "prior" nature of any art cited should the facts support and the situation warrant such an action.

It is believed that this disclosure complies with the requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98, and the Manual of Patent Examining Procedures § 609. If for some reason the examiner considers otherwise, it is respectfully requested that the undersigned be called so that any deficiencies can be remedied.

A copy of each document is enclosed. Some of the documents may have markings thereon. No significance is intended to be attached to the markings.

No item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in § 1.56(c) more than three months prior to the filing of the information disclosure statement. The information cited in the information disclosure statement was cited by the United States Patent Office in one or more applications that are related to the present application.

Also attached hereto is a check in the amount of **$180.00** for the fee set forth in § 1.17(p).

Respectfully submitted,

James W. Huffman
Huffman Law Group, Inc.
Registration No. 35,549
1832 N. Cascade Ave.
Colorado Springs, CO 80907
719.475.7103
719.623.0141 fax
jim@huffmanlaw.net

Date: 12-10-04

"EXPRESS MAIL" mailing label number EL003400736US
Date of Deposit 12-15-04. I hereby certify that this paper is being deposited with the U.S. Postal Service Express Mail Post Office to Addressee Service under 37 C.F.R. §1.10 on the date shown above and is addressed to the U.S. Commissioner of Patents and Trademarks, Washington, D.C. 20231.
By: Cecilia J. Hoy

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary

Sheet 1 of 2

Complete if Known	
Application Number	09/849799
Filing Date	05/04/01
First Named Inventor	G. Glenn Henry Thomas C. McDonald
Group Art Unit	2183
Examiner Name	Tonia Moenske
Attorney Docket Number	CNTR.2052

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.[1]	U.S. Patent Document Number	Kind Code[2]	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AA	5142634		Fite et al	08/25/1992	
	AB	5163140		Stiles et al	11/10/1992	
	AC	5353421		Emma et al	10/04/1994	
	AD	5355459		Matsuo et al	10/11/1994	
	AE	5404467		Saba et al	04/04/1995	
	AF	5530825		Black et al	06/25/1996	
	AG	5687360		Po-Hua Chang	11/11/1997	
	AH	5761723		Black et al	06/02/1998	
	AI	5812839		Hoyt et al	09/22/1998	
	AJ	5850543		Shiell et al	12/15/1998	
	AK	5867701		Brown et al	02/02/1999	
	AL	5948100		Hsu et al	09/07/1999	
	AM	5964868		Gochman et al	10/12/1999	
	AN	5974543		Hilgendorf et al	10/26/1999	
	AO	5978909		Oded Lempel	11/02/1999	
	AP	6044459		Bae et al	03/28/2000	
	AQ	6088793		Liu et al	07/11/2000	
	AR	6108773		Col et al	08/22/2000	
	AS	6151671		D'Sa et al	11/21/2000	
	AT	6314514		Thomas C. McDonald	11/6/2001	
	AU	6502185		Keller et al	12/31/2002	
	AV	6647467		Eric M. Dowling	11/11/2003	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Unique citation designation number. [2]See attached Kinds of U.S. Patent Documents. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST .3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place e check mark here if English language Translation is attached.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary

Sheet 2 of 2

Complete if Known	
Application Number	09/849799
Filing Date	05/04/01
First Named Inventor	G. Glenn Henry Thomas C. McDonald
Group Art Unit	2183
Examiner Name	Tonia Moenske
Attorney Docket Number	CNTR.2052

OTHER PRIOR ART-NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	BA	SAKAMOTO ET AL; Microarchitecture Support for Reducing Branch Penalty in a Superscaler Processor; pp. 208-216; IEEE 1996; Mitsubishi Electric Corp., System LSI Laboratory, 4-1 Mizuhara, Itami, Hyogo 664, Japan.	
	BB	YEH ET AL; ALTERNATIVE IMPLEMENTATION OF TWO-LEVEL ADAPTIVE BRANCH PREDICTION; 19TH Annual International Symposium on Computer Architecture, pp. 124-134, May 19-21, 1992, Gold Coast, Australia.	
	BC	CHANG ET AL; ALTERNATIVE IMPLEMENTATIONS OF HYBRID BRANCH PREDICTORS; Proceedings of MICRO-28, 1995, IEEE.	
	BD	MC FARLING, SCOTT; WRL TECHNICAL NOTE TN-36, "Combining Branch Predictors, June 1993, Western Research Laboratory, 250 University Ave., Palo Alto, CA 94301	
	BE	IEEE 100; THE AUTHORITATIVE DICTIONARY OF IEEE STANDARDS TERMS; Seventh Edition, IEEE, Standards Information Network, IEEE Press,	
	BF	BRAY ET AL; STRATEGIES FOR BRANCH TARGET BUFFERS; Technical Report No. CSL-TR-91-480, June 1991.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Unique citation designation number. [2]Applicant is to place a check mark here if English language Translation is attached.